UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/773,874 | 01/31/2001 | Youngsik Kim | 9898-172 | 7968 |

20575 7590 02/18/2005

MARGER JOHNSON & MCCOLLOM, P.C.
1030 SW MORRISON STREET
PORTLAND, OR 97205

| EXAMINER | |
|---|---|
| MASON, DONNA K | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/773,874 | KIM ET AL. | |
| | Examiner | Art Unit | |
| | Donna K. Mason | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-20,23-27 and 31-33* is/are allowed.

6)☒ Claim(s) *1-8,21,28-30 and 34* is/are rejected.

7)☒ Claim(s) *9-17,22 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. In the Remarks filed November 29, 2004, Applicant asserts that a supplemental Information Disclosure Statement (Form PTO-1449) was included, listing European Patent Application No. 0479702A2, which was previously submitted by Applicant. However, the supplemental Form-1449 listing this application cannot be located in the file. Therefore, the Examiner has listed European Patent Application No. 0479702A2 in the Notice of Reference Cited (Form PTO-892), and the Examiner has considered this reference.

### *Response to Arguments*

2. Applicant's arguments filed November 29, 2004 regarding the 35 USC 102(e) rejection of claims 21 and 34 as being anticipated by U.S. Patent No. 6,738,845 to Hadwiger, et al. ("Hadwiger") have been fully considered but they are not persuasive.

Applicant argues that Hadwiger fails to teach "granting a request by an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block to control only a system bus in an on-chip system", as recited in claims 21 and 34. More specifically, Applicant argues that a request cannot be granted to the mJmCGDMA block because bus 317 (Fig. 3) is dedicated to the mJmCGDMA 318.

However, as shown in Fig. 3, the mJmCGDMA 318 arbitrates for access to system bus 206 and external bus 207. As further described in column 7, lines 16-35

and column 8, lines 1-29, the mJmCGDMA 318 is a bus master which may be selectively connected to the system bus 206 and external bus 207 by way of the arbitration units 315 and 316, as claimed.

Therefore, the Examiner cannot allow claims 21 and 34.

3. Applicant's arguments filed November 29, 2004 regarding the 35 USC 103(a) rejection of claim 5 as being unpatentable over U.S. Patent No. 6,601,126 to Zaidi, et al. ("Zaidi") in view of U.S. Patent No. 5,894,586 to Marks, et al. ("Marks") have been fully considered but they are not persuasive.

Applicant argues that Zaidi in view of Marks does not teach or suggest "a path distinct from the system bus and the external bus" and "a multi-jurisdictional multi-channel general direct memory access block capable of accessing each memory device via the external memory controller and the path, where the path couples the multi-jurisdictional multi-channel general direct memory access block and the external memory controller," as recited in amended claim 5. Applicant points to column 5, lines 14-19, which states that the p-bus (path 124) *is not used to access memory*.

However, as described in column 5, lines 14-24, the cited text regarding the p-bus not being used to access memory, is stated with regard to the CPU —not with regard to the DMA blocks 134 and 138. That is to say, the p-bus (path 124) is the communication interface between the CPU and its peripherals. As further stated in column 5, lines 25-26, the m-bus (system bus 130) is the communications interface between the MAC 140 and the DMA channels (132 and 136). Therefore, the DMA

blocks 134 and 138 use the p-bus (path 124) to access memory, as claimed. (*See also*, column 6, lines 8-10, which states, "If a peripheral block 134 and 138 performs DMA accesses to shared memory, it includes a p-bus interface . . . ").

In the alternative, as shown in Fig. 1, and as described in the 35 USC 103(a) rejection below, Zaidi can be interpreted such that the m-bus 130 is the "path distinct from the system bus and the external bus" and p-bus 124 is the system bus, as claimed. In this way, Zaidi in view of Marks teaches "a multi-jurisdictional multi-channel general direct memory access block capable of accessing each memory device via the external memory controller and the path, where the path couples the multi-jurisdictional multi-channel general direct memory access block and the external memory controller," as claimed.

Therefore, the Examiner cannot allow claim 5.

4. Applicant's arguments (see page 16), filed November 29, 2004, regarding the 35 USC 103(a) rejection of claims 6-8 as being unpatentable over U.S. Patent No. 6,601,126 to Zaidi, et al. ("Zaidi") in view of U.S. Patent No. 5,894,586 to Marks, et al. ("Marks") have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of U.S. Patent Application Publication No. 2001/0032301 to Morita, et al. ("Morita").

The Examiner is persuaded that neither Zaidi nor Marks discloses the features of dependent claims 6-8. However, Morita teaches these claimed features.

Therefore, the Examiner cannot allow claims 6-8.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-4 and 28-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 1 recites the limitation "the first block" in line 9. There is insufficient antecedent basis for this limitation in the claim. The Examiner recommends changing "the first block" in line 9 to --the one of the first blocks-- to be consistent with the previously recited "one of the first blocks" in line 5.

8. Claims 2-4 inherit the deficiencies of independent claim 1.

9. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: a description of the relationship between the first one of the plurality of requests, as recited in line 5, and the external bus. To provide clarity, it is recommended that Applicant add --for using only the external bus-- after "controller" in line 6.

10. Claims 29 and 30 inherit the deficiencies of claim 28.

### *Claim Rejections - 35 USC § 102*

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 21 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,738,845 to Hadwiger, et al. ("Hadwiger").

With regard to claims 21 and 34, Hadwiger discloses an article including: a storage medium (Fig. 3, item 208), said storage medium having stored thereon instructions, that, when executed by at least one device, result in: granting a request by an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block to control only a system bus in an on-chip system; and then granting a request by the mJmCGDMA block to control only an external bus in an off-chip system (*see generally*, Fig. 3, items 200, 317, 318, 205, and 207; column 7, lines 9-12; column 7, lines 65-67; and column 8, lines 1-18).

Therefore, Hadwiger reads on the invention as specified in claims 21 and 34.

### *Claim Rejections - 35 USC § 103*

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,601,126 to Zaidi, et al. ("Zaidi") in view of U.S. Patent No. 5,894,586 to Marks, et al. ("Marks").

With regard to claim 5, Zaidi discloses a device including: a semiconductor chip (Fig. 1, item 102); a system bus on the chip (Fig. 1, item 130); an external bus (Fig. 1, item 104); a path distinct from the system bus and the external bus (Fig. 1, item 124); and a plurality of first blocks on the chip coupled directly with the system bus (Fig. 1, items 132, 134, 138, 136, 140, 142), where at least one of the first blocks is an external memory controller coupled to the external bus and adapted to control at least one memory device that is external to the chip (Fig. 1, item 140); and another one of the first blocks is a direct memory access block that is coupled with the external memory controller via the path (Fig. 1, items 134 and 138).

*In the alternative*, with respect to claim 5, Zaidi discloses a device including: a semiconductor chip (Fig. 1, item 102); a system bus on the chip (Fig. 1, *item 124*); an external bus (Fig. 1, item 104); a path distinct from the system bus and the external bus (Fig. 1, *item 130*); and a plurality of first blocks on the chip coupled directly with the system bus (Fig. 1, items 134, 138, and 140), where at least one of the first blocks is an external memory controller coupled to the external bus and adapted to control at least one memory device that is external to the chip (Fig. 1, item 140); and another one of the first blocks is a direct memory access block capable of accessing each memory device via the external memory controller and the path (Fig. 1, items 134 and 138), where the path couples the direct memory access block and the external memory controller (*see*

Fig. 1, where the path 130 couples the direct memory access blocks 134 and 138 and the external memory controller 140 via channels 132 and 136, respectively).

With regard to claims 6-8, Zaidi further discloses the device where the external memory controller includes: an external bus controller to control the external bus; an address and control multiplexer adapted to receive address and control inputs from both the system bus and the multi-jurisdictional multi-channel general direct memory access block, and adapted to transfer one of the received address and control inputs to the external bus controller; a write data multiplexer adapted to receive data inputs from both the system bus and the multi-jurisdictional multi-channel general direct memory access block and adapted to transfer one of the received data inputs to the external bus controller; and a read data demultiplexer adapted to receive data inputs from the external bus controller, and adapted to transfer the received data inputs to one of the system bus and the chip multi-jurisdictional multi-channel general direct memory access block (*see generally*, column 19, lines 66-67 to column 20, lines 1-3; column 25, lines 36-49; column 4, lines 61-67 to column 5, lines 1-13; column 5, lines 47-65).

Zaidi does not expressly disclose where the direct memory access block is a multi-jurisdictional multi-channel general direct memory access block, as recited in claim 5.

Marks discloses a multi-jurisdictional multi-channel general direct memory access block (Fig. 4, item 20). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the multi-jurisdictional multi-channel general direct memory access block of Marks with the device of Zaidi. The suggestion

or motivation for doing so would have been to improve memory access through use of the multiple channel configuration (column 3, lines 15-18).

Therefore, it would have been obvious to combine Marks with Zaidi to obtain the invention as specified in claim 5.

15. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi in view of Marks as applied to claim 5 above, and further in view of U.S. Patent Application Publication 2001/0032301 to Morita, et al. ("Morita").

As discussed above with regard to the obviousness rejection of claim 5, Zaidi in view of Marks discloses all the features of independent claim 5.

Zaidi in view of Marks does not expressly disclose all the features of dependent claims 6-8.

Morita discloses the well-known features of claims 6-8. Specifically, with regard to claim 6, Morita discloses where an external memory controller includes: an external bus controller (Fig. 1, item 490; paragraph [0052], lines 16-25) to control an external bus (Fig. 2, item 60a) an address and control multiplexer (Fig. 2, item 427a; paragraph [0056]) adapted to receive address and control inputs from both the system bus and the multi-jurisdictional multi-channel general direct memory access block, and adapted to transfer one of the received address and control inputs to the external bus controller; a write data multiplexer (Fig. 2, item 429a; paragraph [0057]) adapted to receive data inputs from both the system bus and the multi-jurisdictional multi-channel general direct memory access block and adapted to transfer one of the received data inputs to the

external bus controller; and a read data demultiplexer (Fig. 2, item 428a; paragraph [0057]) adapted to receive data inputs from the external bus controller, and adapted to transfer the received data inputs to one of the system bus and the chip multi-jurisdictional multi-channel general direct memory access block.

With regard to claim 7, Morita discloses where the address and control multiplexer, the write data multiplexer, and the read data demultiplexer are controlled by inputs from the external bus controller (paragraph [0052]).

With regard to claim 8, Morita discloses where at least one buffer coupled between the external bus controller and the external bus (Fig. 2, items 431a, 432a, 433a, 451a, or 452a).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the external memory controller of Morita with the device taught by Zaidi in view of Marks. The suggestion or motivation for doing so would have been to provide a memory copying method, allowing memory accessing by a processor or peripheral equipment even during execution of memory copying, minimizing overhead by pre-processing for memory copying (paragraph [0012]).

Therefore, it would have been obvious to combine Morita with Zaidi in view of Marks to obtain the invention as specified in claims 6-8.

### ***Allowable Subject Matter***

16. Claims 18-20, 23-27, and 31-33 are allowed.

17. Claims 9-17, 22, and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. Claims 1-4 and 28-30 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

19. The following is a statement of reasons for the indication of allowable subject matter: The primary reason for the allowance of claims 18-20, 23-27, and 31-33 and the allowability of claims 1-4, 9-17, 22, 28-30, and 35 is the inclusion of the limitation "a single on-chip multi-jurisdictional arbiter adapted to receive requests for ownership of the system bus and of the external bus, to rank all the received requests according to a programmable priority schedule, to transmit a first grant signal to the dual [one of first blocks] regarding a first ownership of the external bus and to transmit a second grant signal regarding a second ownership of the system bus to another one of the first blocks that is concurrent with the first ownership" as recited in claim 1.

The prior art is not directed to a system including an arbiter that performs in the manner claimed. More specifically, the prior art does not disclose a system providing concurrent ownership of the external and system buses in the manner claimed.

## *Conclusion*

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM